Wireless Internet on a Chip Technology, Enabled with Integrated Flash Memory

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Agenda

- Technology Scaling
- Wireless Internet on a chip
- Wireless Internet on a chip technology
- Power and performance enhancement
- Cost of integration vs. package solution
- Summary

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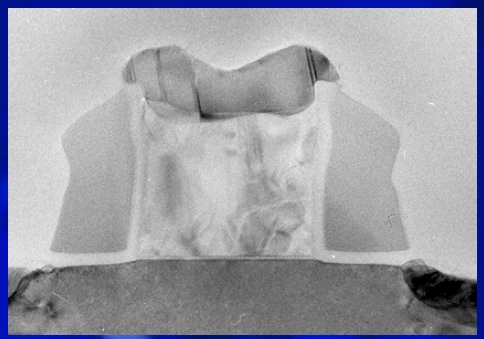
Technology Scaling

- Moore's Law rules
- With the scaling of logic, flash and analog process technologies, it is economical to combine all the capabilities onto a single chip using one manufacturing process.
  - State of art logic transistor technology optimized for performance and low power
  - State of art flash technology optimized for low cost
- Chips produced on the new process will be higher in performance, lower in power at comparable cost

Logic Technology Scaling

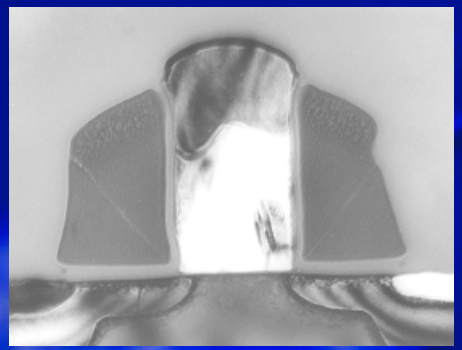
Production Volume Year

1H97



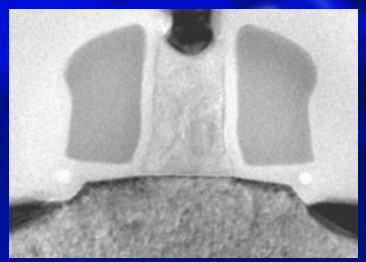
0.20µm

1H99



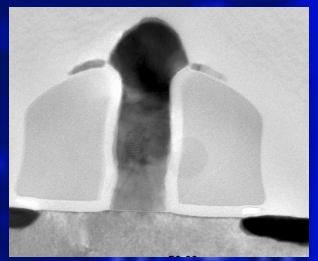
0.13µm

2001



~0.07µm

2003

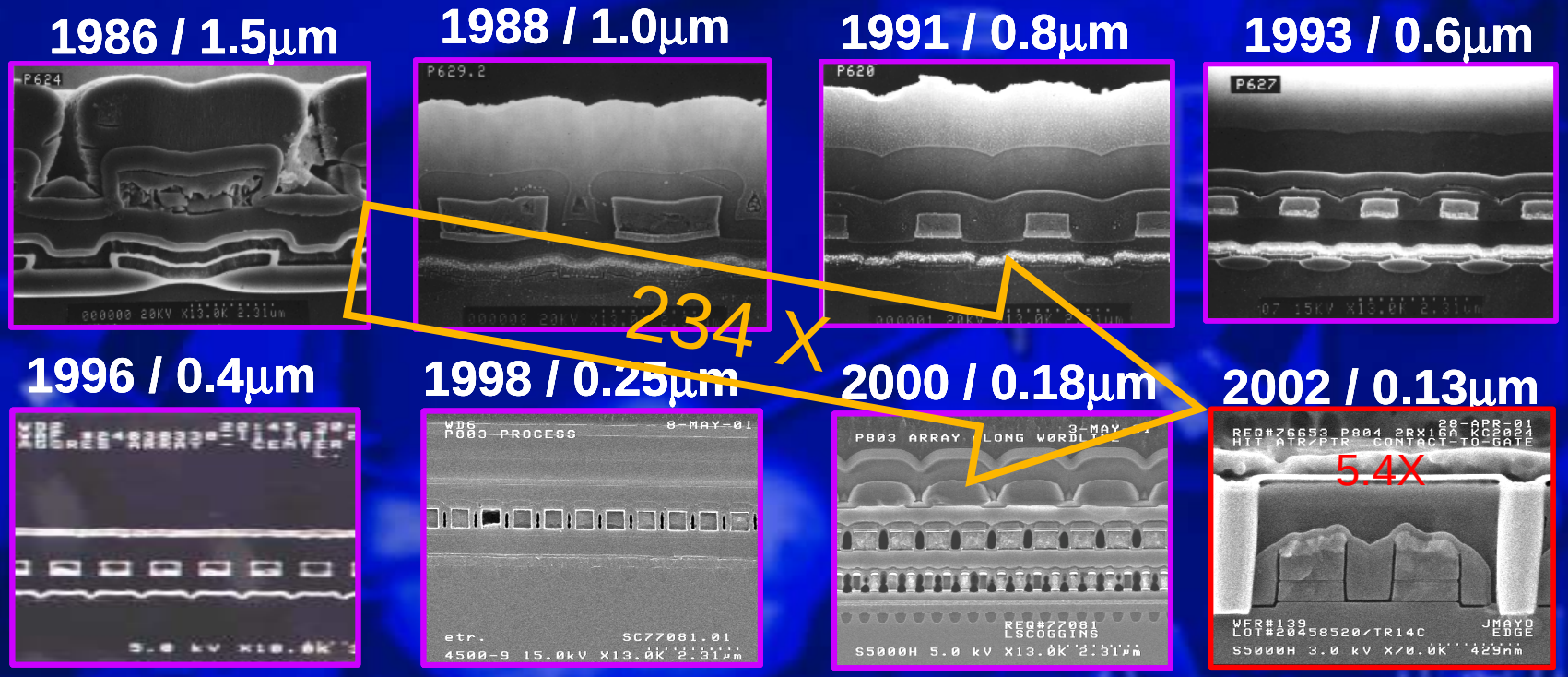


~0.05µm

Gate length

- Driving Moore's Law

ETOX® Technology Scaling



- 18 years and 8 Generations of ETOX® to 0.13 µm

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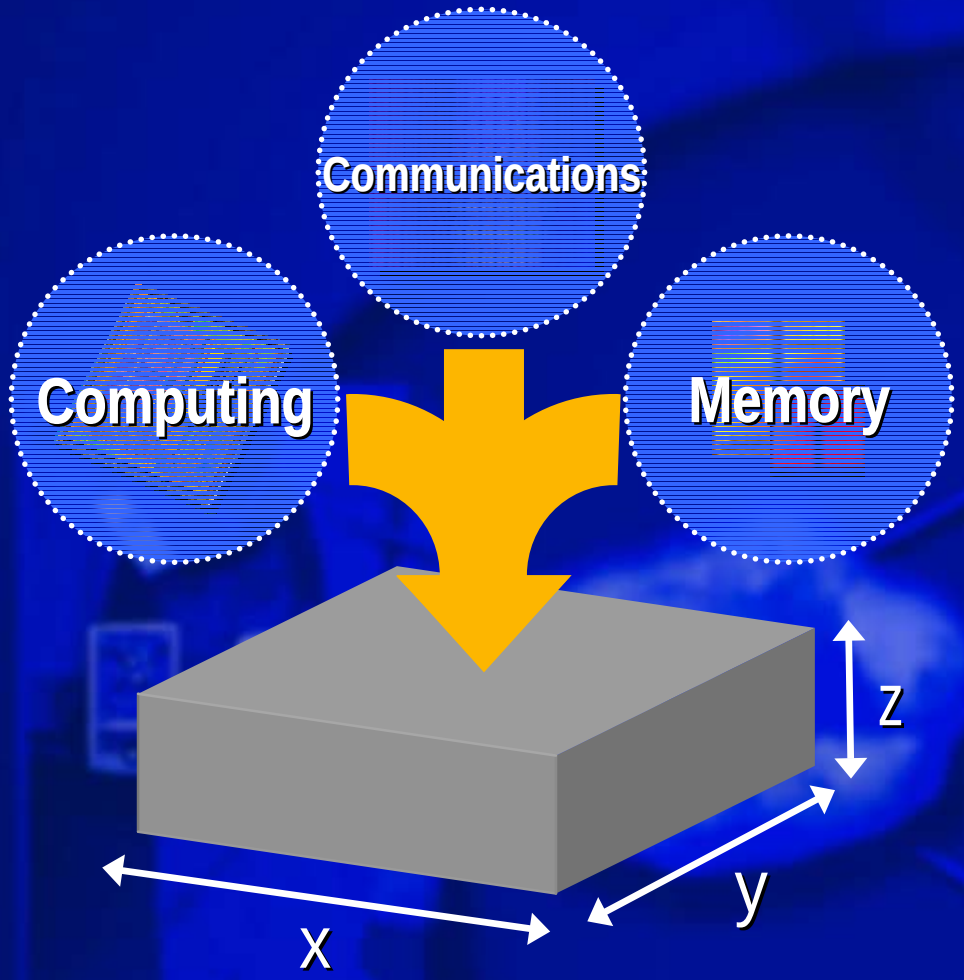
Wireless Internet Requirement

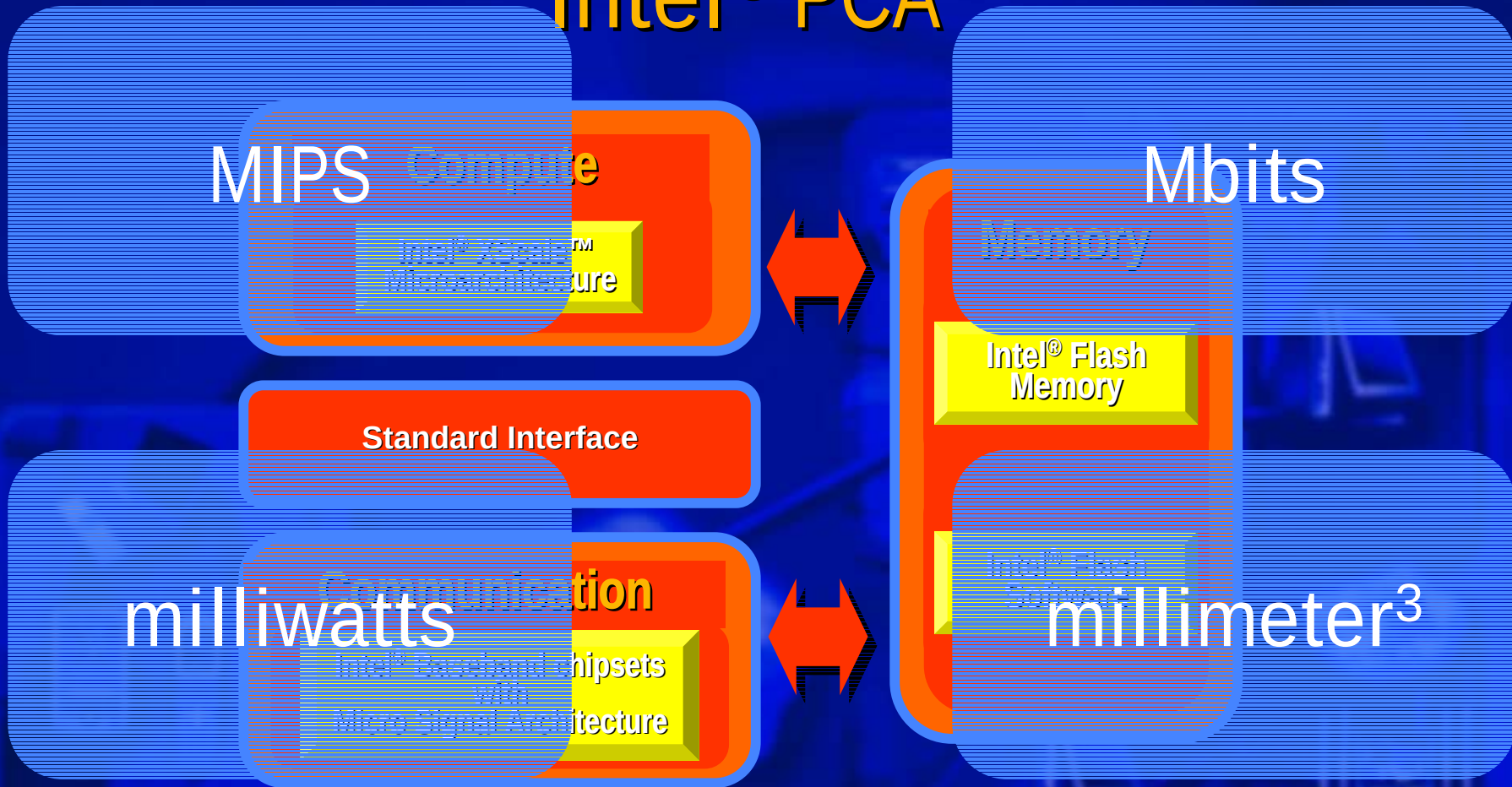
*MIPS * Megabytes / milliwatt & millimeter³*



- **Combination of all functions**
  - **x, y, z dimensions shrinking**
- **Bigger "M's" and smaller "m's" are better**

$$\frac{\text{MIPs}*\text{Megabytes}}{\text{mW}*\text{mm}^3} \rightarrow \infty$$

Intel® PCA


MIPS
Mbits
Standard Interface
milliwatts
millimeter3
Mobility = 2M / 2m
MIPS· Mbit / milliwatt· millimeter3

Current Solution: Different Silicon Processes

Compute

Intel® XScale™ Microarchitecture

Communications

Intel Baseband chipsets With Intel® Micro Signal Architecture

Memory

Intel® Flash Memory

- **Building Blocks: Compute, Communications and Memory**
  - **Silicon Processing: Different process technologies, logic for compute and MSA, mixed signal for analog, and flash for NV memories**

Wireless-Internet-on-a-Chip Technology

Compute

Intel® XScale™ Microarchitecture

Memory

Intel® Flash Memory

Communications

Intel Baseband chipsets With Intel® Micro Signal Architecture

Wireless Internet on a Chip

- Integrating Intel's leadership logic, flash and analog silicon technologies onto the same silicon, without compromising performance or density, providing leadership "System-on-a-Chip" capabilities.
  - Silicon Processing: Exact same process technology steps, same fabrication facility, same wafer → leadership integrated components.

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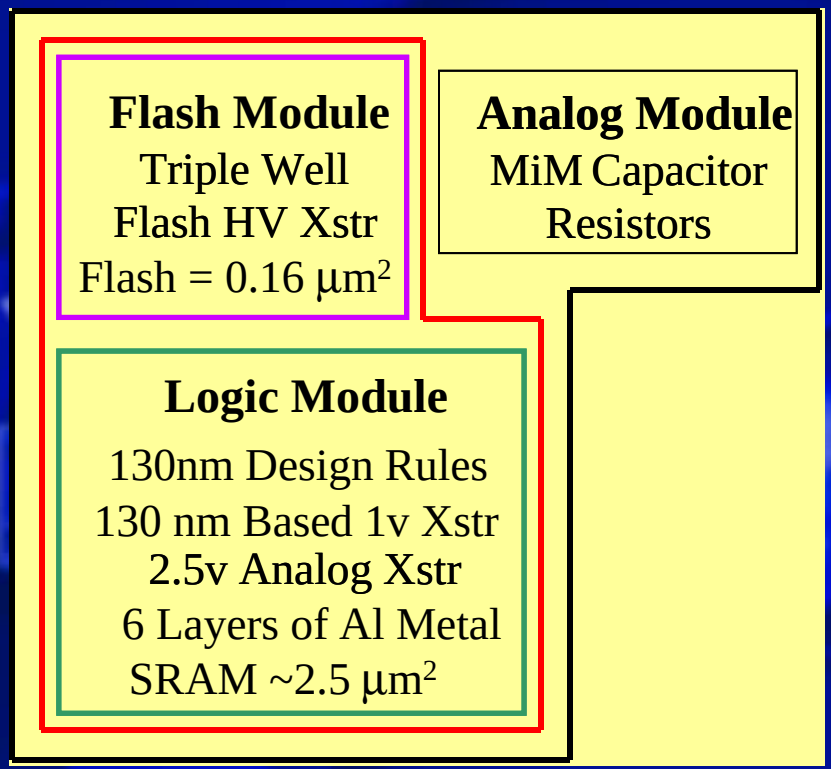
130nm Silicon Platform

Scalable Technology Family Optimized for Internet on a Chip



Logic : Low Cost Logic Technology, focused on Memory Integration, Power, some Analog. Some Slight Density Compromise for Scalability.

Analog : Discretes for Advanced Analog Support

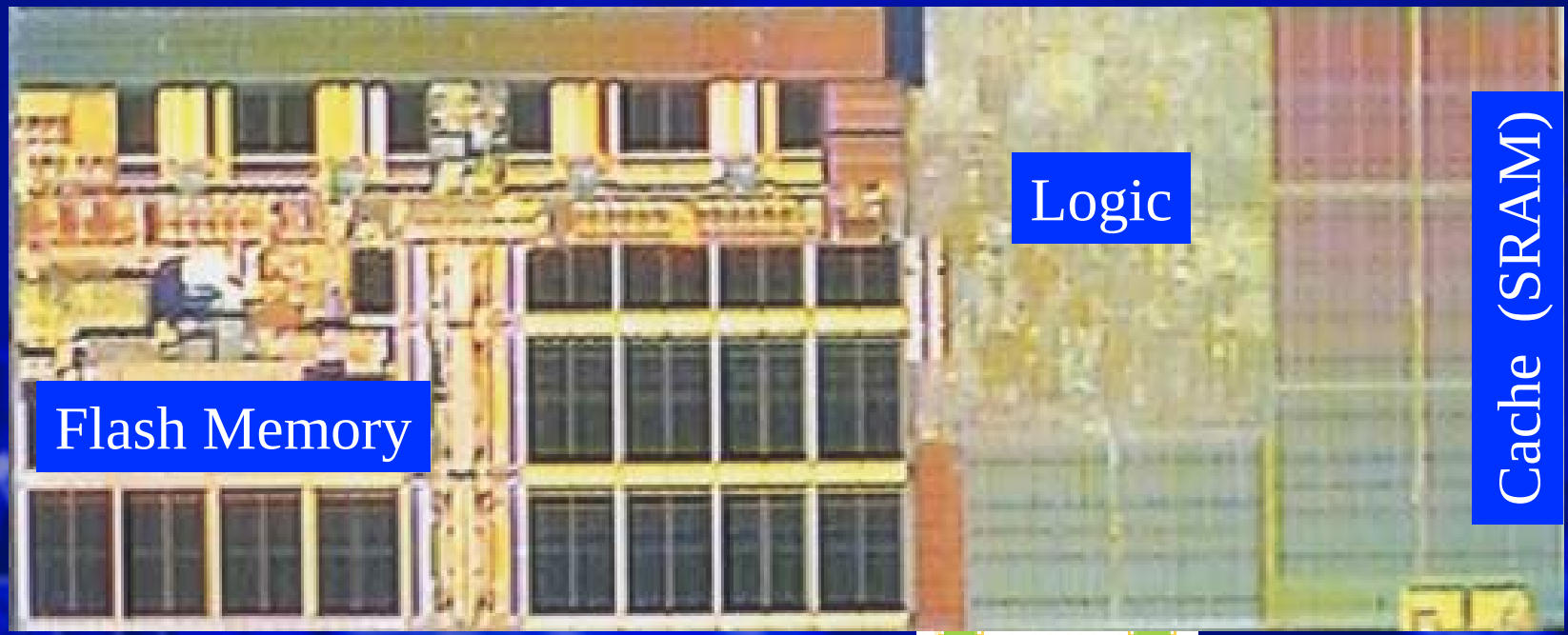
Flash : Lowest Cost Flash Technology, focused on Flash Die Size and High Factory Reuse.

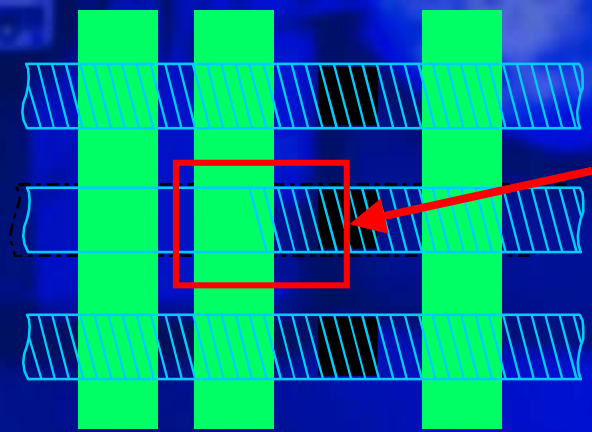
Flash + Logic + Analog
Flash + Logic
Logic + Analog
Logic only
Flash only

Key Technology Features

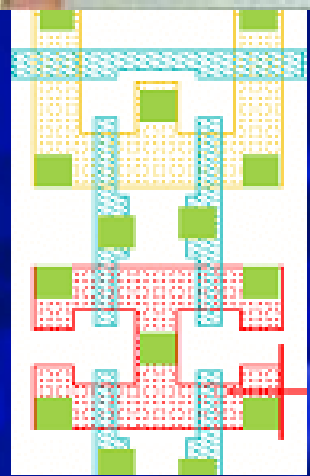
Key Process Modules	Comment
Dual Trench	Allows independent logic and flash isolation
Floating Gate	Self-aligned-floating gate
Quad gate	4 different gate oxides for: flash memory cell; HVT, 3VT, LVT
Gate Patterning	Precision gate patterning for flash and logic
Transistor architecture	HTO Tip spacer, shared wells/tips
Dual Spacer	Creates both High Voltage and Low Voltage spacers
Precision Caps/Resistors	Blocked salicide resistor and MIM capacitor
ULC	Un-landed contact
Aluminum Back End	Al Back end for tight pitch and low cost
Channel Erase	Enables flash cell and HVT xtor scaling
Flash+logic integration	Fully integrated flash+logic technology

Flash + Logic on same Si / Product



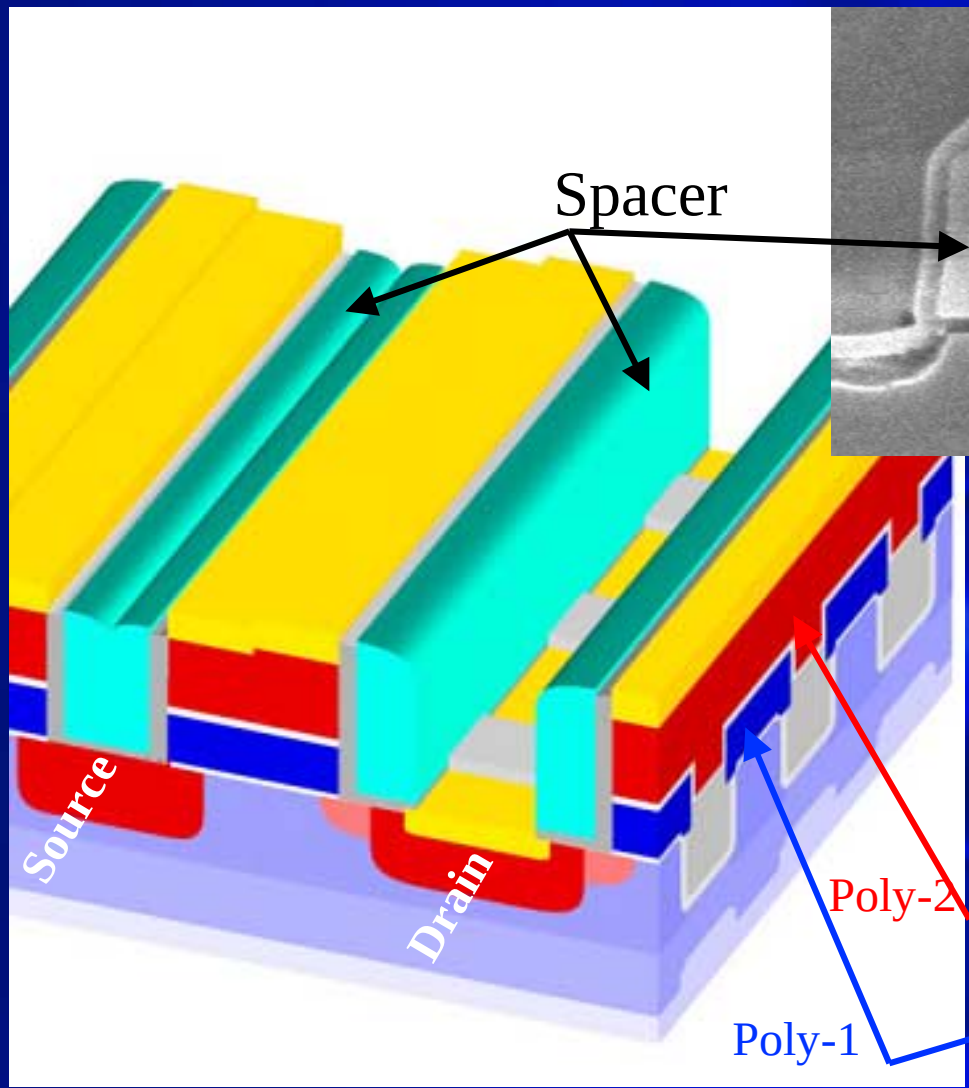


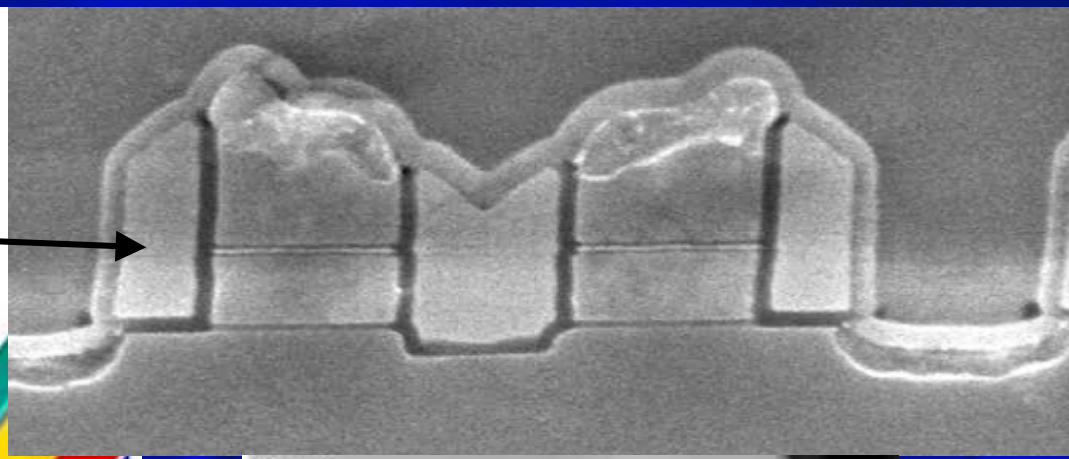
Flash Cell
0.16 um2

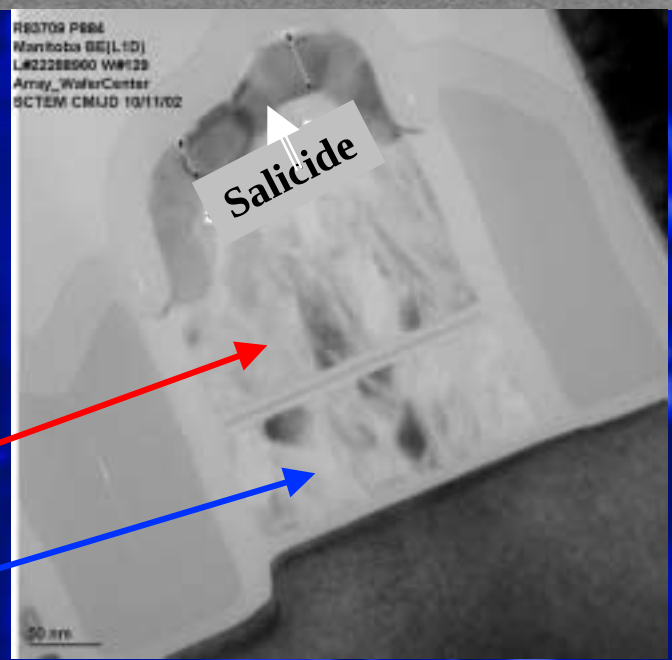


SRAM Cell
2.5 um2

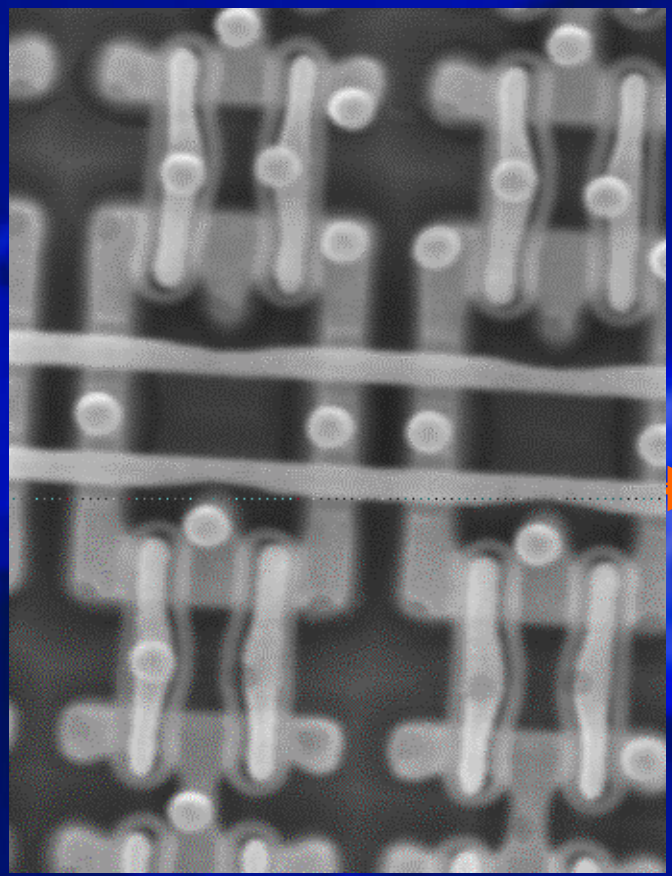
Flash Cell



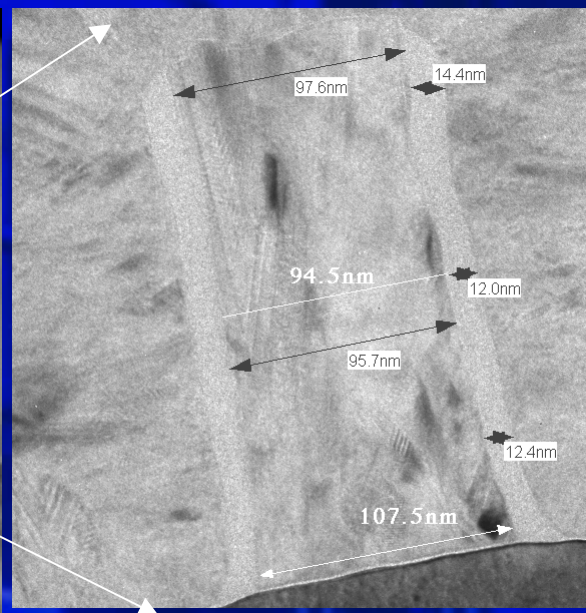




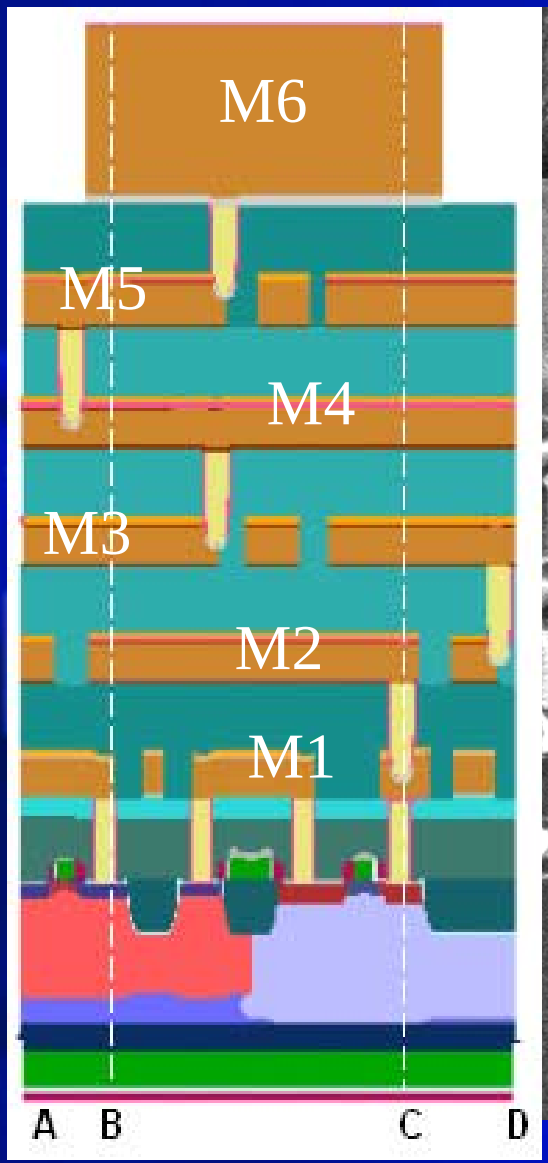
High Density/ High Performance
90nm Poly Gate Transistor for Logic Performance

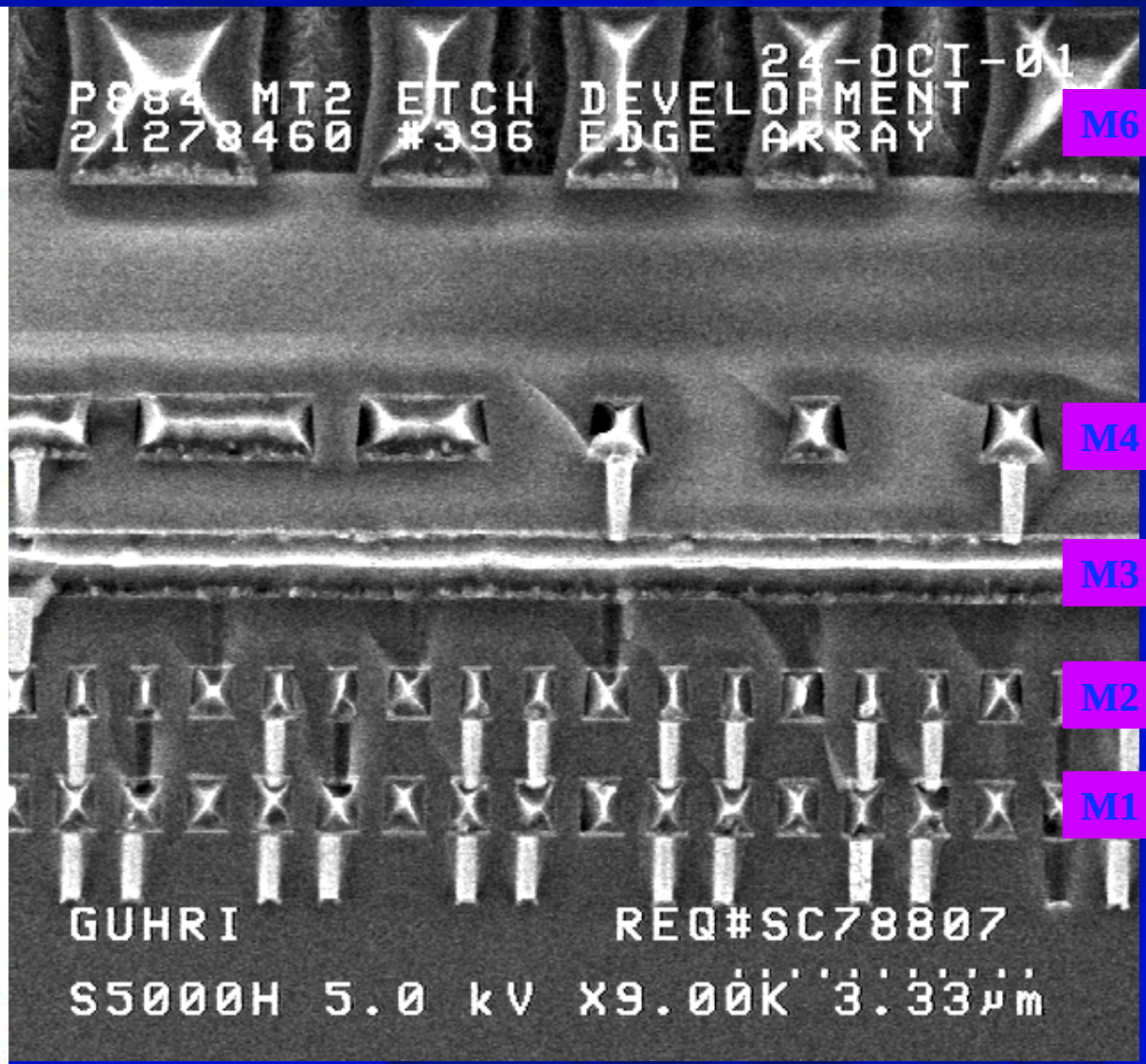


SRAM Cell

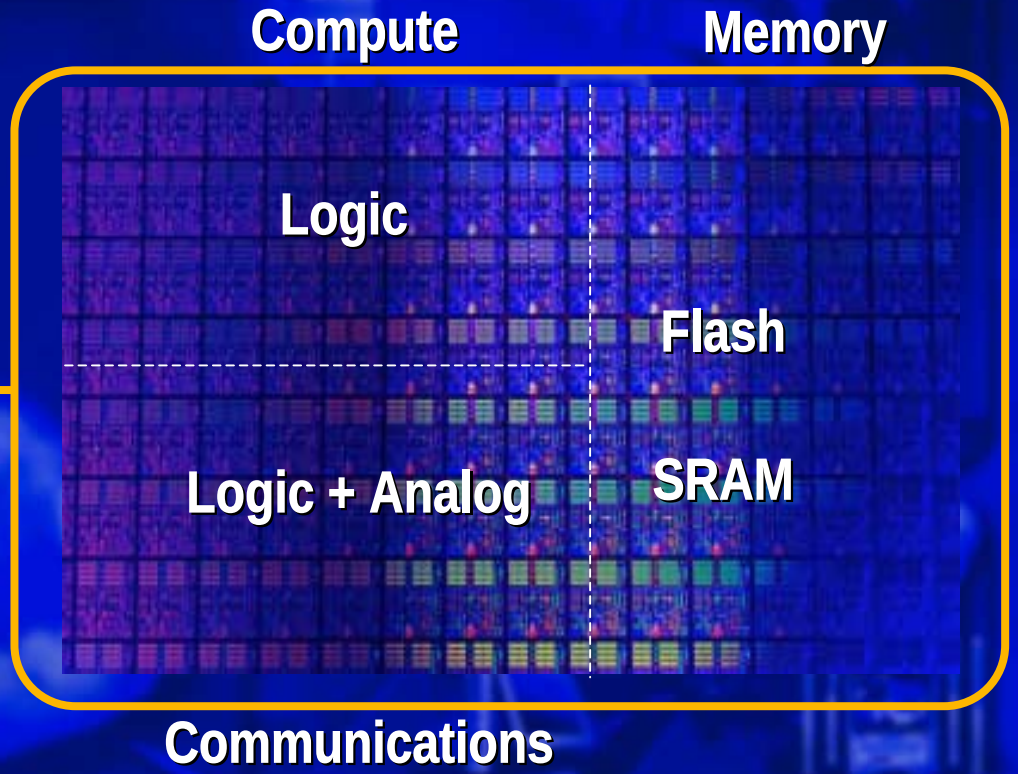


6 Metal (Al) for Logic Density





“Manitoba”
Wireless Internet On-A-Chip



Product samples using Intel 0.13 micron process technology is functional and in validation

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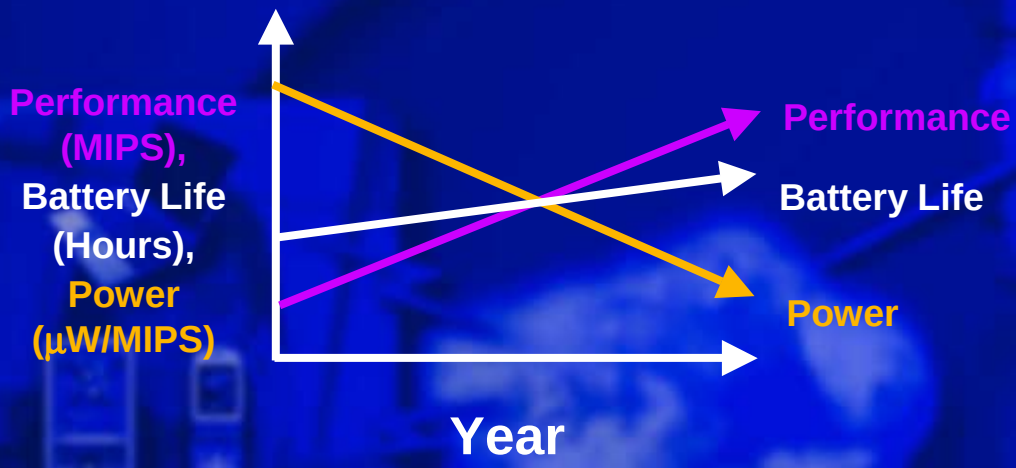
Advantage of Silicon Integration

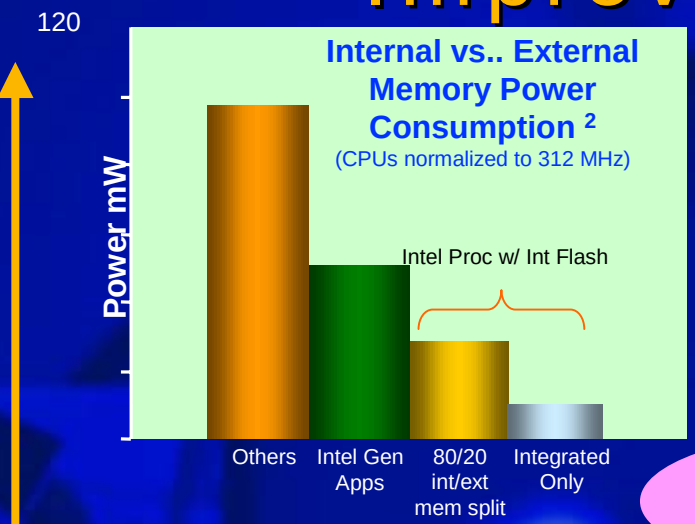
Converged Voice + Data Requirements Trend

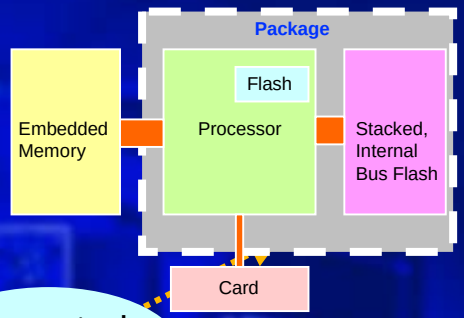


Flash + Logic + Analog Integration

- High Performance with Memory & Compute Integration
- Low Power with elimination of external busses
- Improved µW/MIPS → Longer Battery Life
- Small form factor & improved reliability with fewer components

Integration: Power Performance Improvements





Increasing Battery Life

Integrated Flash

<1V Core
<1v I/O

Internal Priority Code Flash

External Embedded Memory

1.8v Core
1.8-1.5v I/O

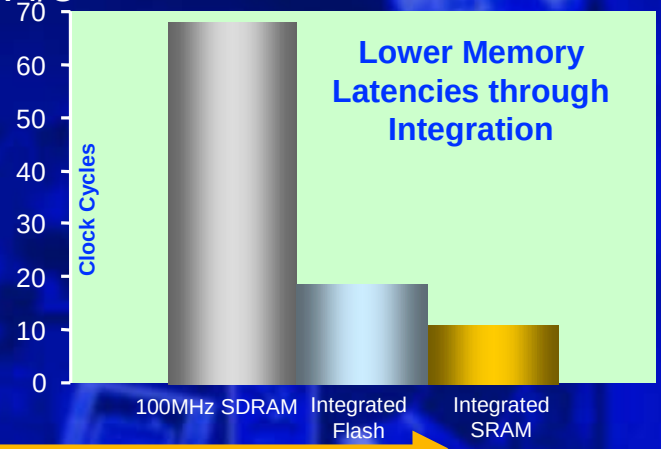
SDRAM Memory

3v > 1.8v Core
1.8v I/O

Card Memory

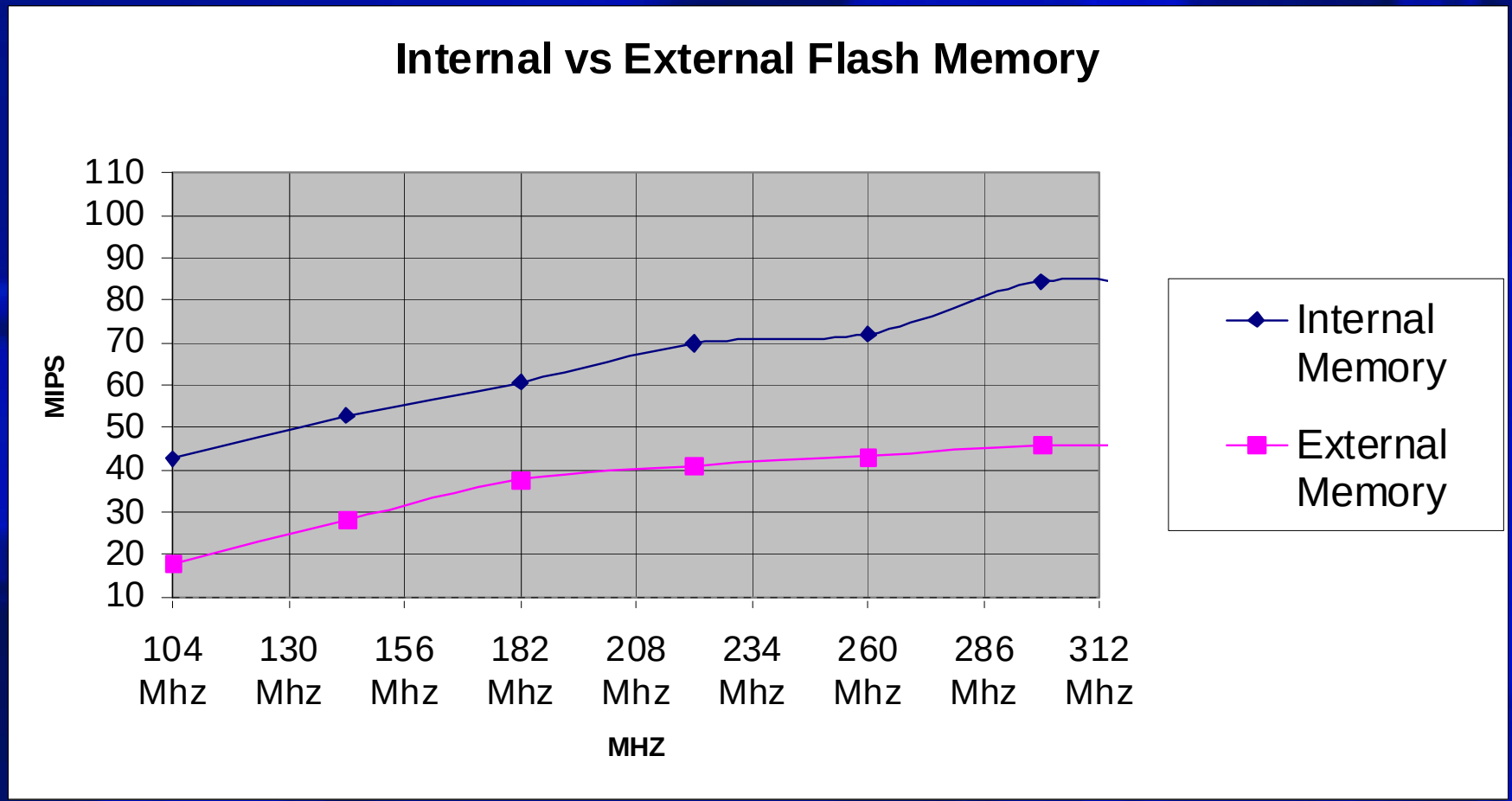
3v Core
3v I/O

1.8v Core
1v I/O



Increasing Performance

Intel ® XScale Core Performance (Simulation)



As Cache hit rate drops, MIPs for apps drops for external flash memory

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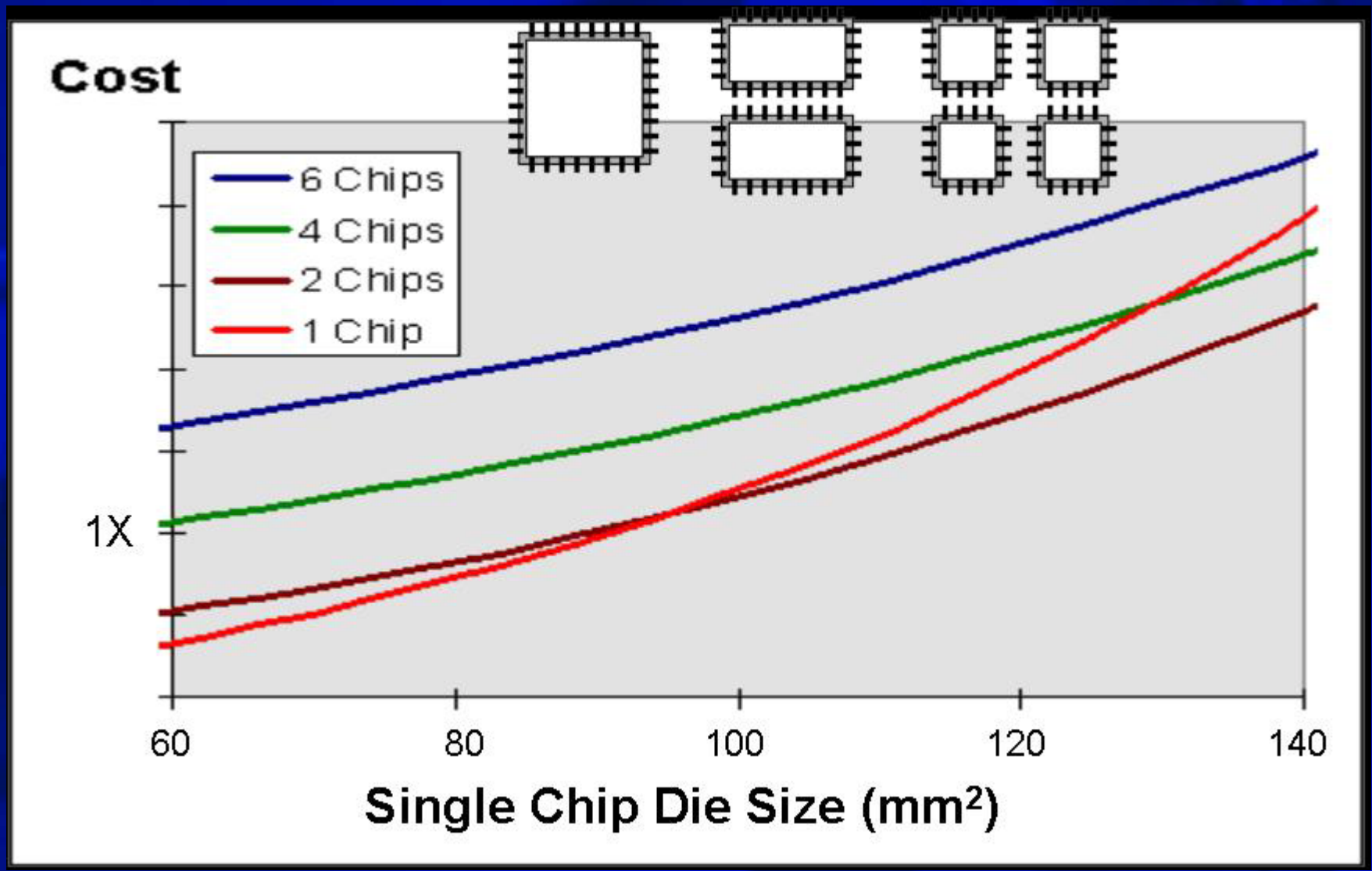
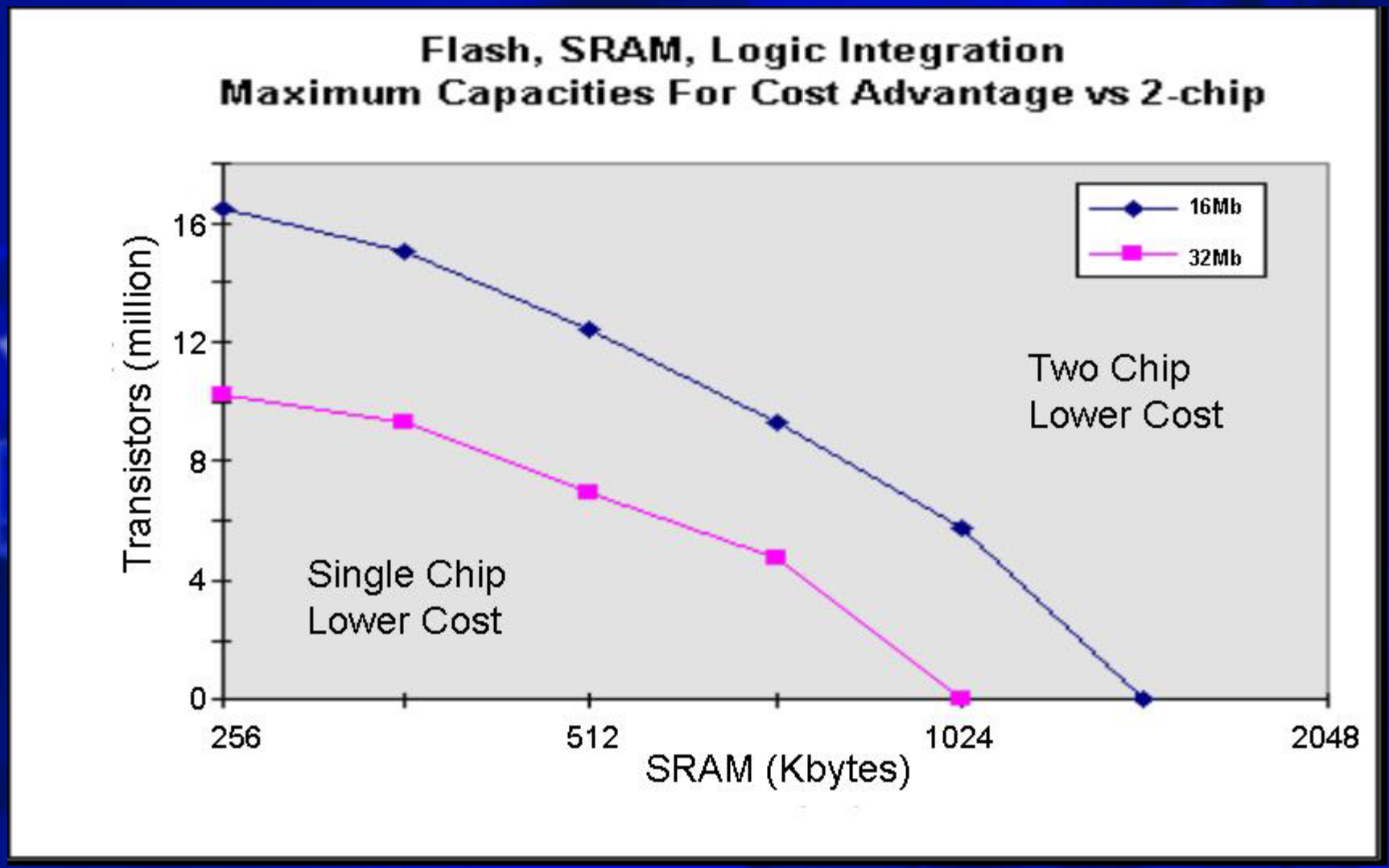
Integration vs. Multichip Package Cost Consideration



Memory and Logic Density Cost for Single Chip vs. 2 Chip (0.13 µm)



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- **Moore's law drives continuous scaling, enabling cost effective integration of advanced transistors with advanced flash memories**
- **Advanced process capability enables the integration of application processor, MSA, baseband logic, flash and SRAM on a chip: *internet on a chip***
- **Integration of memory improves performance and lowers power consumption**
- **Integration is cost effective for smaller die sizes**
- **High performance, low power cellular products are possible with this new capability**